REMARKS

A. Background

The present amendment is filed in response to the Examiner's Office Action mailed November 16, 2004. Claims 1-10, 22-25, and 32-34 were pending. Claims 11-21 and 26-31 were previously withdrawn from consideration. Claims 1, 22, and 33 are amended. New Claims 35 and 36 are added. Claims 1-10, 22-25, and 32-36 are now pending in view of the above amendments.

Reconsideration is respectfully requested in view of the above amendments and following remarks. For the Examiner's convenience and reference, Applicant's remarks are presented in the order in which the corresponding issues were raised in the Office Action.

B. Rejections Under 35 U.S.C. § 103

The Office Action rejects claims 1, 4, 6-8, 22, 23, 25, and 32-34 under 35 U.S.C. § 103(a) as being unpatentable over United States Patent No. 5,300,799 to Nakamura, *et al.* ("*Nakamura*") in view of United States Patent No. 5,877,054 to *Yamauchi*. As will be shown below, however, *Nakamura* and *Yamauchi* – assuming *arguendo* that they qualify as references under Section 103 – fail to teach or suggest, either alone or in combination, each and every element of the pending claims, and thus do not make obvious the present claimed invention. Note that a general description of the teachings of *Nakamura* and *Yamauchi* has been provided in previous submissions by the Applicant.

The present claimed invention is substantially distinct from the devices taught by *Nakamura* and *Yamauchi*. Specifically, amended independent claim 1 requires, in a single transistor ferroelectric memory cell, the presence of a semiconductor substrate having a source and a drain that is spaced apart from the source, wherein the source is "sized and configured to

comprise the source of the ferroelectric memory cell *and the source of an adjacent ferroelectric memory cell.*" Neither *Nakamura* nor *Yamauchi* disclose such a memory cell structure. Indeed, though *Nakamura* discloses source/drain diffusion regions 5 that are shared by neighboring transistors FC1-FC8 (*Nakamura*, col. 6, ll. 57-58; col. 8, ll. 4-5), no one source/drain diffusion region serves as a source for adjacent memory cells, as required by amended claim 1. In other words, the source/drain diffusion regions of *Nakamura* "serve for both of a source and a drain" (*Nakamura*, col. 3, l. 66), *i.e.*, as a source for one of the transistors FC1-FC8, *but as a drain* for the neighboring transistor. (*See also* col. 7, ll. 13-19, which state that the number of transistors constituting the memory cell of *Nakamura* can be arbitrarily selected. Applicant submits that this requires the use of each source/drain diffusion region as a source for one transistor and a drain for an adjacent transistor in order to preserve source/drain parity for each transistor.) Thus, *Nakamura* is devoid of any teaching of a source serving as the source for adjacent memory cells, as required by claim 1.

Similarly, *Yamauchi* also fails to teach or suggest all required elements of amended claim 1. In particular, *Yamauchi* teaches, as shown in Figure 2A, a diffusion layer 2 that is "shared by two adjacent memory cells," col. 12, l. 14. Importantly, however, the diffusion layer includes a "drain diffusion layer 2a *for one of the two adjacent memory cells . . .* and a source diffusion layer 2b *for the other memory cell...*," col. 12, ll. 10-13 (emphasis added). Thus, as was the case with *Nakamura* above, the source of *Yamauchi* is not shared between adjacent memory cells, as explicitly required in amended claim 1, but is dedicated to only one memory cell. It is noted that this independent source relationship is shown not only in Figure 2A, but in various other figures of *Yamauchi*, including Figures 27-28.

In light of the above discussion, Applicant submits that at least the above recited elements of amended claim 1 are neither taught nor suggested, either alone or in combination, by

Nakamura or *Yamauchi*. Applicant therefore submits that a *prima facie* case of obviousness does not exist with respect to independent claim 1 in view of the cited references, and respectfully requests that rejection of the claim under Section 103 be removed. Moreover, inasmuch as claims 2-10 are dependent upon independent claim 1, Applicant submits that these claims are also allowable for at least the reasons given above.

Amended independent claims 22 and 33 are also patentably distinct for at least the reasons given above. In particular, claim 22 discloses a ferroelectric memory cell requiring "a single source that serves as the source for both the ferroelectric memory cell and an adjacent ferroelectric memory cell." Similarly, claim 33, which discloses a ferroelectric memory cell, requires "a source that serves both as the source for the ferroelectric memory cell and the source of an adjacent memory cell." Again, these limitations are found neither in *Nakamura* nor *Yamauchi*. Thus, claims 22 and 33, as well claims 23-25 and 34 that respectively depend therefrom, are allowable.

The Office Action also rejects certain claims with respect to various cited references. In particular, claims 2 and 24 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Nakamura/Yamauchi* in view of United States Patent No. 5,506,748 to Hoshiba. Claim 3 is rejected under Section 103(a) as being unpatentable over *Nakamura/Yamauchi* in view of United States Patent No. 6,100,558 to Krivokapic, *et al.* Claim 5 is rejected under Section 103(a) as being unpatentable over *Nakamura/Yamauchi* in view of a publication entitled "Introduction to Microelectronic Fabrication, Volume V," by Richard C. Jaeger. Claim 9 is rejected under Section 103(a) as being unpatentable over *Nakamura/Yamauchi* in view of United States Patent No. 6,339,008 B1 to Takenaka, and claim 10 is rejected under Section 103(a) as being unpatentable over *Nakamura/Yamauchi* in view of United States Patent No. 6,172,392 B1 to Schmidt, *et al.*

Applicant notes that each of the above rejections is at least partly based on the *Nakamura* and *Yamauchi* references. Applicant further notes that each of the rejected claims as set forth above is ultimately dependent one of the amended independent claims 1, 22, and 33. As was previously discussed, the teachings of *Nakamura* and *Yamauchi* are inapplicable to the present invention as applied to claims 1, 22, and 33 for failing to teach or suggest each of the limitations contained in those claims. Thus, *Nakamura* and *Yamauchi* are inapplicable to the present claims rejected under Section 103 for at least the above reasons, that is, their failure to teach or suggest all of the claim limitations contained not only in independent claims 1, 22, or 33, but also the limitations contained in the presently rejected dependent claims. Thus, the Office Action has failed to establish a *prima facie* case of obviousness. Applicant therefore respectfully submits that claims 2, 3, 5, 9, 10, 24, and the other dependent claims are allowable and that the above rejections under Section 103 should be withdrawn.

C. **New Claims**

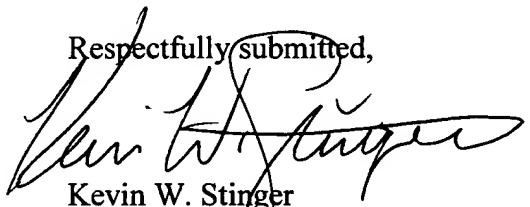
Applicant further submits that new claims 35-36 are also allowable in light of the cited references. In particular, new independent claim 35 discloses a ferroelectric memory cell array that includes first and second ferroelectric memory cells that are positioned adjacent one another on a semiconductor substrate, and "a source defined in the semiconductor substrate that is configured for use as the source for both the first and second ferroelectric memory cells." Because, as discussed above, neither *Nakamura* nor *Yamauchi* teaches any such device, Applicant respectfully submits that claim 35 and its dependent claim 36 are allowable. Entry and allowance of these claims is therefore respectfully solicited.

CONCLUSION

In view of the discussion and amendments submitted herein, Applicant respectfully submits that each of the pending claims 1-10, 22-25, and 32-36 is now in condition for allowance. Therefore, reconsideration of the rejections is requested and allowance of those claims is respectfully solicited. In the event that the Examiner finds any remaining impediment to a prompt allowance of this application that can be clarified in a telephonic interview, the Examiner is respectfully requested to initiate the same with the undersigned attorney.

Dated this 15th day of March, 2005.

Respectfully submitted,



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